AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

28. (Currently Amended) A processor, comprising:

multiple programmable ~~engines~~ units integrated within the processor; and

~~circuitry~~ logic integrated within the processor to map resources within the multiple ~~engines~~ units into a single address space.

29. (Currently Amended) The processor of claim 28, wherein the resources within the multiple programmable ~~engines~~ units comprise registers within the multiple programmable ~~engines~~ units.

30. (Currently Amended) The processor of claim 28, wherein the single address space comprises addresses corresponding to shared resources external to the multiple programmable ~~engines~~ units.

31. (Currently Amended) The processor of claim 30, wherein the shared resources external to the multiple programmable ~~engines~~ units comprise at least one ~~of~~ selected from the following group: a memory internal to the processor, a randomly accessible memory external to the processor, and a Peripheral Component Interconnect (PCI) unit.

32. (Currently Amended) The processor of claim 28, wherein the multiple programmable ~~engines~~ units comprise multiple programmable multi-threaded ~~engines~~ units.

33. (Originally) The processor of claim 28, further comprising an interface to a media access controller (MAC).

34. (Currently Amended)The processor of claim 28, wherein the ~~circuitry~~ logic comprises ~~circuitry~~ logic to receive a command from a programmable processor other than the multiple programmable ~~engines~~ units.

35. (Currently Amended) The semiconductor chip of claim 34, wherein the programmable processor other than the multiple programmable ~~engines~~ units comprises a programmable processor integrated within the processor.

36. (Currently Amended) A method, comprising:

mapping an address in a single address space to a resource within one of a set of multiple programmable ~~engines~~ units integrated within a processor, the single address space including addresses for different ones of the resources in different ones of the multiple programmable ~~engines~~ units.

37. (Original) The method of claim 36, further comprising receiving a command specifying the address in the single address space.

38. (Currently Amended) The method of claim 37, wherein the command comprises one ~~of~~ selected from the following group: a read command and a write command.

39. (Currently Amended) The method of claim 37, wherein the receiving the command comprises receiving the command from a programmable processor other than one of the multiple programmable ~~engines~~ units.

40. (Original) The method of claim 39, wherein the programmable processor comprises a programmable processor integrated within the processor.

41. (Currently Amended) The method of claim 36, wherein the resource within the one of the set of multiple programmable ~~engines~~ units comprises at least one register.

42. (Currently Amended)The method of claim 36, wherein the single address space comprises addresses corresponding to shared resources external to the multiple programmable ~~engines~~ units

43. (Currently Amended) The method of claim 36, wherein the multiple programmable ~~engines~~ units comprise multiple programmable multi-threaded ~~engines~~ units.

44. (Currently Amended) A device, comprising:

at least one ~~Ethernet~~ media access controller (MAC); and

at least one processor coupled to the at least one ~~Ethernet~~ media access controller, the processor comprising:

multiple programmable multi-threaded ~~engines~~ units; and

~~circuitry~~ logic to map resources within the multiple ~~engines~~ units and resources external to the multiple engines into a single address space, the resources within the multiple engines comprising registers, the resources external to the multiple ~~engines~~ units comprising at least one Random Access Memory (RAM) external to the processor.

45. (Currently Amended)The device of claim 45, wherein the processor further comprises a programmable processor integrated within the processor, the programmable processor having a different architecture than the multiple ~~engines~~ units.